Listing of the Claims:

The following is a complete listing of all the claims in the application, with an indication of the status of each:

1. (Currently Amended) A coprocessor coupled to a main processor having an execution speed greater than that of said coprocessor, the coprocessor comprising:

a two-dimensional array of processing cells, including a plurality of periphery cells located on peripheral sides of the array; and

an interface module surrounding the two-dimensional array of processing cells, comprising:

a plurality of input/output ~~input/ouput~~ (I/O) pads for the coprocessor,

a plurality of border cells disposed along an outside of the two-dimensional array and surrounding the two-dimensional array, each border cell being connected to a corresponding one of the periphery cells, each border cell including a buffer connected to the corresponding one of the periphery cells, and

a crossbar network for reconfigurably connecting each of the I/O pads to a selectable one of the border cells,

wherein the buffer of each border cell connects to the corresponding one of the periphery cells and connects through the crossbar network to the I/O pad connected to the border cell.

2. (Previously Presented) The coprocessor of claim 1, wherein the array comprises a systolic processing array.

3. (Canceled).

4. (Currently Amended) The coprocessor of claim 1, wherein each processing cell of a plurality of the processing cells is connected by a respective plurality of four paths to corresponding four of said processing cells and the coprocessor is capable of performing ~~performs~~ mathematical operations having a ~~whose~~ timing ~~is~~ based on a flow of ~~input~~ operands along the paths.

5. (Currently Amended) The coprocessor of claim 1, wherein the processing cells ~~inter-cell connection~~ within the array are arranged in rows and columns such that one processing cell is interconnected to other of said processing cells such that said one processing ~~each~~ cell ~~of the array~~ is connected only to processing cells whose column is the same and whose row is immediately adjacent, and only to processing cells whose row is the same and whose column is immediately adjacent.

6. (Currently Amended) A coprocessing system including the coprocessor, interface module and main processor of claim 1 and a shared memory ~~memnory~~ that communicatively connects with the interface module and the main processor to provide the main processor to coprocessor connection.

7. (Canceled)

8. (Currently Amended) The coprocessor of claim 1, wherein said two-dimensional array of processing cells, said a plurality of periphery cells located on peripheral sides of the array and said interface module are formed within an [[An]] integrated circuit ~~comprising the coprocessor of claim 1~~.

9-12. (Canceled).

13. (Currently Amended) A functional unit comprising: ~~having~~

a main processor;

a two-dimensional array of processing cells ~~and being~~ coupled to the [[a]] main processor, the processing cells comprising non-periphery cells and periphery cells surrounding the non-periphery cells; and ~~, the unit having~~

a mechanism external to the two-dimensional array for reconfiguring a plurality of intra- processor information paths to the array to respective said periphery cells only.

14. (Canceled).

15. (Previously Presented) The unit of claim 13, wherein inter-cell connection within the array is such that each cell of the array is connected only to cells whose column is the same and whose row is immediately adjacent, and only to cells whose row is the same and whose column is immediately adjacent.

16. (Previously Presented) The unit of claim 13, further including means for transmitting a plurality of array programs to corresponding predetermined subsets of said processing cells.

17. (Previously Presented) A system including the functional unit of claim 16, and an array program generator for generating the array programs to be transmitted, and, when needed, updating a program, transmitting the updated program, and transmitting concurrently, when needed, a reconfigure signal to said mechanism to correspondingly update a current steady state connection pattern of said information paths.

18. (Previously Presented) The system of claim 17, further including a compiler configured for receiving, in response to said program updating, data representative of input and output timing for said unit and further configured for compiling an instruction based on said data.

19. (Canceled).

20. (Currently Amended) A method for interfacing a coprocessor to a main processor, comprising the steps of:

configuring the coprocessor to comprise a two-dimensional array of processing cells and to have an execution speed greater than that of said processor, the processing cells comprising non-periphery cells and periphery cells surrounding the non-periphery cells;

communicatively connecting each of the non-periphery cells only to the processing cells that are immediately ~~immediatly~~ neighboring the non-periphery cell; and

communicatively connecting the periphery cells to said processor by an interface module having a mechanism for reconfiguring a plurality of information paths between the interface module and respective said periphery cells.

21. (Currently Amended) The coprocessor of claim 1, wherein said configuring the coprocessor configures the array in a ~~is~~ rectangular arrangement, wherein the periphery consists of those of said processing cells located in all of a first row, last row, first column and last column of said array, and wherein the interface module's mechanism for reconfiguring a plurality of information

paths reconfigures information paths directly connecting the interface module and each of the cells on the periphery of the array.

22. (Previously Presented) The coprocessor of claim 1, wherein the interface comprises a plurality of border cells directly connected to the respective processing cells on the periphery of the array.

23. (Currently Amended) The coprocessor of claim 1, further comprising a master cell for forwarding array programs to the processing cells of the two-dimensional ~~dimenstional~~ array.

24. (Currently Amended) The functional unit of claim 13, wherein the mechanism for reconfiguring the plurality of intra-processor information paths to the array to respective cells on the periphery of the array comprises:

a plurality of input/output ~~input/ouput~~ (I/O) pads for the functional unit,

a plurality of border cells disposed along an outside of the two-dimensional array, each border cell being connected to a corresponding one of the periphery cells, each border cell including a buffer, and

a crossbar network for reconfigurably connecting each of the I/O pads to one of the border cells.

25. (Currently Amended) The method of claim 20, wherein said communicatively connecting the coprocessor to said processor by an interface module having a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array comprises:

providing a plurality of input/output ~~input/ouput~~ (I/O) pads for the coprocessor,

providing a plurality of border cells disposed along an outside of the two-dimensional ~~dimentional~~ array, each border cell being connected to a corresponding one of the periphery cells, each border cell including a buffer, and

employing a crossbar network to reconfigurably connect each of the I/O pads to one of the border cells.